REMARKS

Applicant is in receipt of the Office Action mailed April 12, 2004. Claims 1, 10, 30, 41, 43, 50, 61, and 62 have been amended. Further consideration of the present case is earnestly requested in light of the following remarks.

Applicant appreciates the allowance of the matter of claims 32, 33, 36-40, and 52-60, but believes that the claims as currently written are allowable, as argued below.

Section 112 Rejections

Claims 1-21, 24-31, 34, 35, and 44-51 were rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Office Action rejected claims 1, 61, and 62, citing the phrase "a corresponding P memory medium" as being indefinite. Applicant first notes that the actual phrase recited in these claims is "a corresponding P memory medium*s*" (*emphasis added*). Applicant has amended these claims to clarify the meaning of 'P', specifically, that 'P' is an integer greater than one. Thus, for example, if P equals eight, then the phrase in question means "a corresponding eight memory mediums", where the eight memory mediums correspond respectively to the eight processors.

Applicant has amended claims 41 and 43 to address the antecedent basis error of claim 43.

The Office Action rejected claims 4, 11, 24, 31, 44, and 51, citing the phrases "a first mirror processor" and "a second mirror processor" as being indefinite. Applicant respectfully submits that the term "mirror processor", specifically the first mirror processor of claim 4, is clearly described on page 15, lines 8-15, which reads:

> "In one embodiment, each processor i_p has corresponding mirror processor $P-i_p-1$. Thus, for example, processor 1 has mirror processor P-2. Conversely, processor P-2 has mirror processor 1. Therefore, each processor exchanges data with its mirror processor.
> Said another way, every processor may copy $n_b-1 = N/P-1$ elements, starting from the element with local index 1 (i.e. all local

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elements except the first one) into a buffer buf_0. During the same operation, each processor may also determine its mirror processor as the processor whose index is $P-i_p-1$. A second buffer buf_1 of the same length as buf_0 may be allocated by every processor to store data received from its mirror processor."

In other words, for various operations performed in the method, each processor of the P processors is paired with, or operates in conjunction with, another of the P processors, referred to as a "mirror processor".

Similarly, the "second mirror processor" of claim 4 is clearly described on page 15, lines 23-26, which reads:

"each processor i_p of the P processors may receive an element of the local vector of a corresponding second mirror processor. In one embodiment, the second mirror processor for processor i_p has index $P-i_p$. In other words, the second mirror processor may be the processor just subsequent to the mirror processor of 422."

Applicant respectfully submits that the term "mirror processor" is clearly defined in both the specification and the claims, noting that the particular index designations for a given processor's mirror processors are specifically provided in dependent claims 7 and 8 (and corresponding claims 27 and 28).

Applicant respectfully requests removal of the section 112 rejection of claims 1-21, 24-31, 34, 35, and 44-51.

Section 103 Rejections

The Office Action rejected claims 1-3, 21-23, 41-43, 61, and 62 under 35 U.S.C. 103(a) as being unpatentable over Tsutsui (U.S. 5,349,549, "Tsutsui") in view of Ju et al. (U.S. 6,304,887, "Ju"). Applicant respectfully disagrees.

As the Examiner is certainly aware, to establish a prima facie obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce

the claimed invention, absent some teaching or suggestion or incentive to do so. In re Bond, 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). As held by the U.S. Court of Appeals for the Federal Circuit in Ecolochem Inc. v. Southern California Edison Co., an obviousness claim that lacks evidence of a suggestion or motivation for one of skill in the art to combine prior art references to produce the claimed invention is defective as hindsight analysis.

In addition, the showing of a suggestion, teaching, or motivation to combine prior teachings "must be clear and particular . . ... Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence'." *In re Dembiczak,* 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). The art must fairly teach or suggest to one to make the specific combination as claimed. That one achieves an improved result by making such a combination is no more than hindsight without an initial suggestion to make the combination.

Applicant submits that neither Tsutsui nor Ju provides a motivation to combine, and so the combination of Tsutsui and Ju is improper. Moreover, Applicant submits that even if Tsutsui and Ju were properly combinable, which Applicant argues they are not, the resulting combination would not produce Applicant's invention as claimed.

Amended claim 1 recites:

1. (Currently Amended) A method for performing parallel computation of a Discrete Transform of an input signal x, wherein the method operates in a system comprising P interconnected processors and a corresponding P memory mediums, wherein P is an integer greater than one, the method comprising:

receiving the input signal x, wherein the input signal x comprises N elements, wherein N is evenly divisible by $4*P^2$;

the P interconnected processors executing a preprocess in parallel on the signal x to produce a first intermediate vector y;

the P interconnected processors executing a real-to-complex Fourier Transform on said first intermediate vector y to produce a second intermediate vector a; and .

the P interconnected processors executing a post-process in parallel on the second intermediate vector a to produce a result vector v, wherein the result vector v comprises the Discrete Transform of the input signal x;

wherein the Discrete Transform of the signal x is useable in analyzing the signal x.

Applicant notes that Tsutsui discloses a signal processing method wherein the processing operations for performing an MDCT (modified discrete cosine transform) and an IMDCT (inverse modified discrete cosine transform) are carried out using an FFT with a shorter length, to reduce the number of processing operations, such as the number of multiplications and the number of additions, to reduce the work area required, and to achieve a higher operating speed. (Col. 4, lines 57-65). More specifically, Tsutsui describes a mathematical simplification for computing an MDCT and IMDCT more efficiently, where the length of the FFT computed is reduced from N to N/4.

This is in direct contrast with Applicant's system as represented in amended claim 1. For example, nowhere does Tsutsui teach or describe performing parallel computation of a Discrete Transform of an input signal x in a system comprising P interconnected processors and a corresponding P memory mediums, where P is an integer greater than one, and where the input signal x comprises N elements, where N is evenly divisible by $4*P^2$.

In fact, the only mentions Tsutsui makes of distributed computation are in column 17, lines 26-30 (referring to FIG. 3), and column 18, lines 18-22 (referring to FIG. 5) which read:

> "The circuit shown in FIG. 3/5 can be realized using discrete circuitry, or multiple microprocessors. Preferably, however, the majority of processing operations are performed using an appropriately programmed digital signal processor circuit and auxiliary memories."

Thus, Tsutsui's method does not depend on a specified relationship between the number of signal elements and the number of processors/memory mediums used to compute the transform.

The Office Action asserts that Tsutsui discloses "executing a Fourier transform (S01) on vector y to produce a second intermediate vector a". However, Applicant notes that Tsutsui's execution of the Fourier transform is a *complex-to-complex* Fourier transform, as described in column 5, lines 13-16. In contrast, amended claim 1 includes the limitation of a *real-to-complex* Fourier Transform being applied to vector y to generate vector a. Thus, Applicant's vector y is real-valued, and vector a is complex, while Tsutsui's vectors are both complex.

Thus, Applicant submits that Tsutsui neither teaches nor suggests the above-described limitations of claim 1. Applicant further submits that Tsutsui teaches away from Applicant's invention as represented in claim 1 in that Tsutsui's method specifically reduces the length of the FFT computed from N to N/4, while Applicant's invention as represented in claim 1 does not.

The Office Action admits that Tsutsui fails to teach the discrete transform being performed in parallel in a system comprising P interconnected processors and corresponding memory mediums, but asserts that Ju discloses a parallel processing system including P interconnected processors and corresponding memory mediums for partitioning the input signal into P ordered local vectors and distributing the local vectors to the memory mediums, and performing a transform in parallel as claimed by Applicant. Applicant respectfully disagrees.

Ju discloses a DSP (digital signal processor) for performing FFT computations with low latency by parallel processing of complex data points through a plurality of butterfly FFT execution units, specifically employing a single address generator for all of the memory units coupled to like ports on each execution unit. (Abstract)

Nowhere does Ju teach or suggest performing parallel computation of a Discrete Transform of an input signal x in a system comprising P interconnected processors and a corresponding P memory mediums, where P is an integer greater than one, and where the input signal x comprises N elements, where N is evenly divisible by $4*P^2$.

Additionally, as described above, Ju's system applies the FFT (via the plurality of butterfly FFT execution units) to complex data, and thus, like Tsutsui, Ju's Fourier

Transform is a *complex-to-complex Fourier Transform*, in contrast to the *real-to-complex Fourier Transform* of claim 1.

Thus, Applicant respectfully submits that neither Tsutsui nor Ju, either singly or in combination, teaches or suggests all of the features and limitations of Applicant's invention as represented in claim 1. Thus, for at least the reasons provided above, Applicant submits that claim 1 and those claims dependent thereon are patentably distinct and non-obvious over Tsutsui in view of Ju, and are thus allowable.

Independent claims 21, 41, 61, and 62 include similar limitations as claim 1, and so the above arguments apply with equal force to these claims. Thus, claims 21, 41, 61, and 62, and claims respectively dependent thereon, are similarly patentably distinct and non-obvious over Tsutsui in view of Ju, and are thus allowable for at least the reasons provided above.

Removal of the 103 rejection of claims 1-3, 21-23, 41-43, 61, and 62 is respectfully requested.

Applicant also asserts that numerous ones of the dependent claims recite further distinctions over the cited art. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5181-77600/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard
☒ Notice of Change of Address

Respectfully submitted,

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